37452
37461
74595
88399

Final | COM'L: H-10/15/25, Q-15/25 MIL: H-20/25

PALCE16V8

EE CMOS 20-Pin Universal Programmable Array Logic

Advanced Micro Devices

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DISTINCTIVE CHARACTERISTICS

- Pin, function and fuse-map compatible with all 20-pin GAL® devices
- Electrically erasable CMOS technology provides reconfigurable logic and full testability
- High speed CMOS technology
  - 10 ns propagation delay for "-10" version
  - 15 ns propagation delay for "-15" version
  - 25 ns propagation delay for "-25" version
- Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series
- Outputs programmable as registered or combinatorial in any combination
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Cost-effective 20-pin plastic DIP and PLCC packages
- Programmable on standard device programmers
- Supported by PALASM® software
- Fully tested for 100% programming and functional yields and high reliability

GENERAL DESCRIPTION

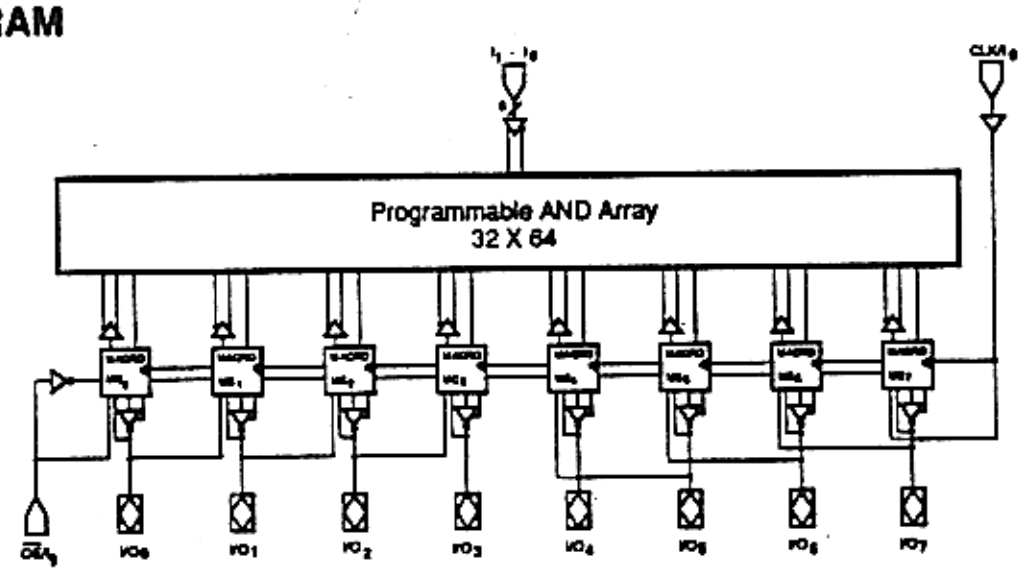
The PALCE16V8 is an advanced PAL® device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM



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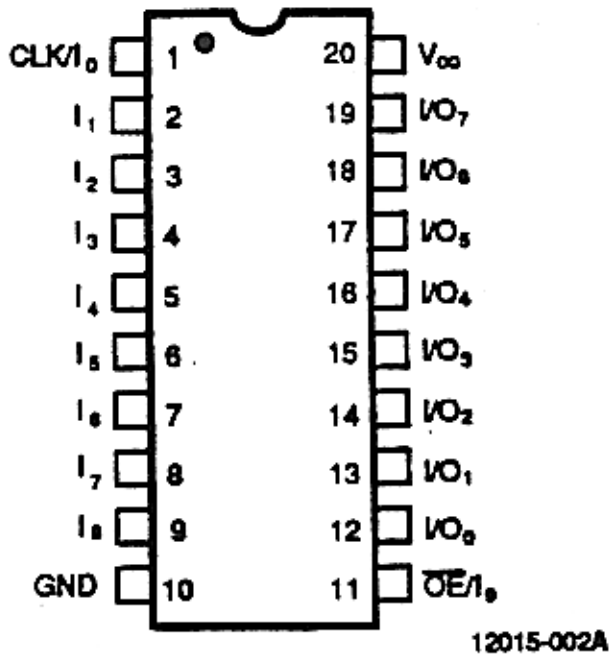
Publication # 12015 Rev. C Amendment
Issue Date: January 1990

CONNECTION DIAGRAMS
Top View

DIP



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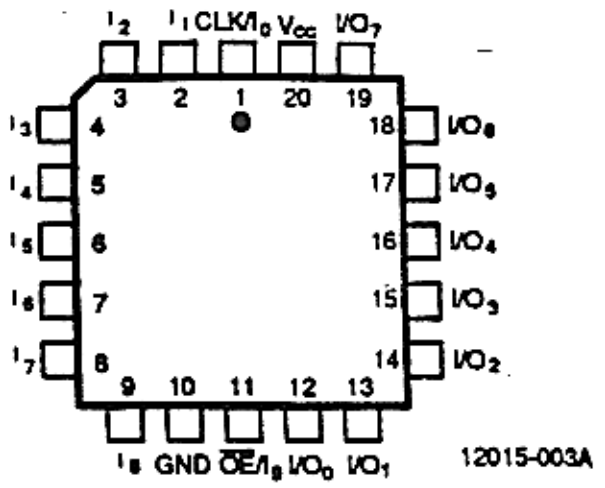
PLCC/LCC



12015-003A

Note: Pin 1 is marked for orientation

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Flip-Flops
f. Power
g. Speed
h. Package Type
i. Operating Conditions
j. Programming Designator

PAL CE 16 V 8 H -15 P C

a. **FAMILY TYPE**
PAL = Programmable Array Logic

b. **TECHNOLOGY**
CE = CMOS Electrically Erasable

c. **NUMBER OF ARRAY INPUTS**

d. **OUTPUT TYPE**
V = Versatile

e. **NUMBER OF FLIP-FLOPS**

f. **POWER**
H = Half Power (90 mA Icc)
Q = Quarter Power (55 mA Icc)

g. **SPEED**
-10 = 10 ns t_{PD}
-15 = 15 ns t_{PD}
-25 = 25 ns t_{PD}

h. **PACKAGE TYPE**
P = 20-Pin Plastic DIP (PD 020)
J = 20-Pin Plastic Leaded Chip Carrier (PL 020)

i. **OPERATING CONDITIONS**
C = Commercial (0°C to +75°C)

j. **PROGRAMMING DESIGNATOR**
Blank = Initial Release
/4 = First Revision
(May require different programmer revisions)

Valid Combinations		
PALCE16V8H-10	PC, JC	Blank, /4
PALCE16V8H-15		
PALCE16V8H-25		
PALCE16V8Q-15		
PALCE16V8Q-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

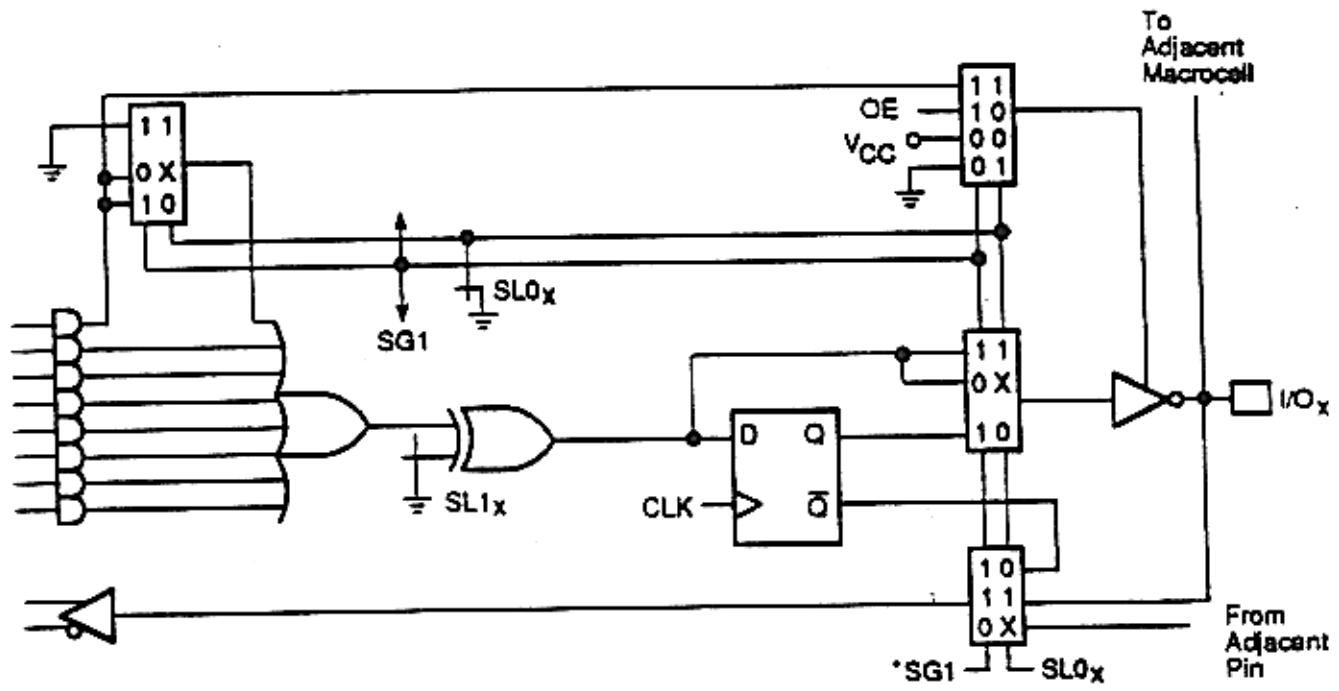
FUNCTIONAL DESCRIPTION

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



*In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

12015-004B

PALCE16V8 Macrocell

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA)	H		90	mA
		V_{CC} = Max., f = 15 MHz	Q		55	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min.	-10 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input or Feedback to Clock			10		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{CF}	Clock to Feedback (Note 3)					ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	55.5		MHz
		Internal Feedback	$1/(t_S+t_{CF})$			MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

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